

SPECULATIVE REGISTER ADJUSTMENT

ABSTRACT

Sub  
A6  
In one embodiment, a programmable processor is adapted  
to include a speculative count register. The speculative  
5 count register may be loaded with data associated with an  
instruction before the instruction commits. However, if  
the instruction is terminated before it commits, the  
speculative count register may be adjusted. A set of  
counters may monitor the difference between the speculative  
10 count register and its architectural counterpart.